Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1A**
2. **2A**
3. **2B**
4. **2C**
5. **2D**
6. **2Y**
7. **GND**
8. **1Y**
9. **1D**
10. **1E**
11. **1F**
12. **1B**
13. **1C**
14. **VCC**

**.055”**

**12 11 10 9**

**13**

**1**

**2 3 4 5**

**8**

**7**

**6**

**14**

**.051”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: GND or FLOAT**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .051” X .055” DATE: 8/17/21**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54ALS51**

**DG 10.1.2**

#### Rev B, 7/1